Notice of Allowability	Application No.	Applicant(s)	
	10/568,842	GOESSEL ET AL.	
	Examiner	Art Unit	
	Guerrier Merant	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *08/11/04*.

2. ☒ The allowed claim(s) is/are *41-80, renumbered as 1-40*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 02/17/06
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *05/20/10* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

1. This communication is responsive to 08/11/04. Claims 41-80 are presented for examination.

Oath/Declaration

2. The Oath/Declaration filed 07/14/08 complies with the requirements set forth in MPEP 602 and therefore is accepted.

Information Disclosure Statement

3. The information disclosure statement (IDS) submitted on 02/17/06 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Priority

4. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d) of German Application No. 10338922.9, filed on 08/20/03.

EXAMINER'S AMENDMENT

5. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Gleason Mark on 05/20/10.

The application has been amended as follows:

Claim 41: An electrical diagnostic circuit for the testing and/or the diagnostic analysis of an integrated circuit comprising:

a plurality of external inputs (E_n) for receiving digital values;

a plurality of essentially similar, series-connected switching units comprising:

each switching unit is connected to one external input

for receiving a test signal of an integrated circuit;

each switching unit has an internal input for an input

signal from a switching unit arranged upstream or downstream,

the switching units are configured to be controllable such that an input signal present at the internal input of a switching unit, in dependence on a control signal of the switching unit, ~~are~~ is forwarded either unchanged to the internal input of the switching unit arranged downstream or to the circuit output and/or are fed back to an internal input of a switching unit arranged upstream, or are combined with the test signal in each case present at the external input and the combination value determined from this combination is forwarded to the internal input of the switching unit in each case arranged downstream or to the circuit output and/or is fed back to the internal input of one of the ~~a~~ switching unit<u>s</u> arranged upstream; and

a circuit output for outputting an output value.

Claim 52: An electrical diagnostic circuit for the testing and/or the diagnostic analysis of an integrated circuit comprising:

a plurality of external inputs (E.sub.n) for receiving digital values;

a plurality of essentially similar, series-connected switching units comprising: each switching unit is connected to one external input for receiving a test signal of an integrated circuit;

each switching unit has an internal input for an input signal from a switching unit arranged upstream or downstream,

the switching units are configured to be controllable such that an input signal present at the internal input of a switching unit, in dependence on a control signal of the switching unit, ~~are~~ is forwarded either unchanged to the internal input of the switching unit arranged downstream or to the circuit output and/or are fed back to an internal input of a switching unit arranged upstream, or are combined with the test signal in each case present at the external input and the combination value determined from this combination is forwarded to the internal input of the switching unit in each case arranged downstream or to the circuit output and/or is fed back to the internal input of one of the ~~a~~ switching units arranged upstream; and

a circuit output for outputting an output value comprising wherein the first switching unit has an AND gate and a storage unit and in that all further switching units

have one gate each, particularly an exclusive OR gate (XOR.sub.2-XOR.sub.n), one multiplexer each and one storage unit each.

Claim 62: A method for testing and/or for the diagnostic analysis of an integrated circuit, comprising:

providing an electrical diagnostic circuit which has n external inputs for receiving test data of n parallel datastreams of an integrated circuit to be tested and/or to be diagnosed and which is capable of generating signatures from the received test data, the test data present at the n external inputs selectively being included or not included in the generation of the signatures,

connecting the electrical diagnostic circuit to the integrated circuit to be tested and/or to be diagnosed, in such a manner that the n inputs of the electrical diagnostic circuit are present at the n outputs of the integrated circuit;

controlling the switching units of the electrical diagnostic circuit in such a manner that the test data in each case present at the external inputs are included in the generation of the signatures;

detecting and processing the test data of the integrated circuit to be tested and/or to be diagnosed to form at least one signature in one or in more successive test runs through the electrical diagnostic circuit;

checking the signature for correctness ~~by means of the test~~ by comparing the signatures determined in the test with the correct signature stored in the tester or determined by the tester;

if at least one errored signature has been determined, carrying out the following processes:

performing k successive test runs, wherein in each case only those data, present at the external input ~~E~~$_i$, of the n datastreams in the jth run are included in the compacting in the electrical diagnostic circuit if the binary coefficient $a_{i,j}$ of the equations for determining the control points of a linear separable error-correcting code with n information points $u_1, ..., u_n$ and with k control points $v_1, ..., v_k$ is equal to one, the k control points $v_1, ..., v_k$ being determined by the k binary equations

$$v_1 = a_{1,1}\, u_1 \oplus ... \oplus a_{1,n} u_n$$

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$$v_1 = a_{k,1} u_1 \oplus ... \oplus a_{k,n} u_n$$

from the n information points.

~~Determining~~ determining the errored elements in the n datastreams, particularly the errored scan cells of the diagnosed integrated circuit from the deviations of ~~the~~ observed output signatures y^b output by the electrical diagnostic circuit at its output in the k test runs

$$[y_1^b, y_2^b, y_3^b, ...]$$

from the corresponding correct output signatures $\underline{y}^k$

$[y_1^k, y_2^k, y_3^k, \ldots]$

where n, k, j and y are integers greater or equal to 1 (n, k, j, y ≥ 1).

Claim 76: A tangible storage medium comprises a computer program for testing an integrated circuit comprising:

providing an electrical diagnostic circuit which has n external inputs for receiving test data of n parallel datastreams of an integrated circuit to be tested and/or to be diagnosed and which is capable of generating signatures from the received test data, the test data present at the n external inputs selectively being included or not included in the generation of the signatures,

connecting the electrical diagnostic circuit to the integrated circuit to be tested and/or to be diagnosed, in such a manner that the n inputs of the electrical diagnostic circuit are present at the n outputs of the integrated circuit;

controlling the switching units of the electrical diagnostic circuit in such a manner that the test data in each case present at the external inputs are included in the generation of the signatures;

detecting and processing the test data of the integrated circuit to be tested and/or to be diagnosed to form at least one signature in one or in more successive test runs

through the electrical diagnostic circuit;

checking the signature for correctness ~~by means of the test~~ by comparing the signatures determined in the test with the correct signature stored in the tester or determined by the tester;

if at least one errored signature has been determined, carrying out the following processes:

performing k successive test runs, wherein in each case only those data, present at the external input ~~E~~$_i$, of the n datastreams in the jth run are included in the compacting in the electrical diagnostic circuit if the binary coefficient $a_{i,j}$ of the equations for determining the control points of a linear separable error-correcting code with n information points u_1, ..., u_n and with k control points v_1, ..., v_k is equal to one, the k control points v_1, ..., v_k being determined by the k binary equations

$$v_1 = a_{1,1}\, u_1 \oplus \ldots \oplus a_{1,n} u_n$$

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$$v_1 = a_{k,1} u_1 \oplus \ldots \oplus a_{k,n} u_n$$

from the n information points.

~~Determining~~ determining the errored elements in the n datastreams, particularly the errored scan cells of the diagnosed integrated circuit from the deviations of ~~the~~

observed output signatures $\underline{y}^b$ output by the electrical diagnostic circuit at its output in the k test runs

$$[y_1^b, y_2^b, y_3^b, \ldots]$$

from the corresponding correct output signatures $\underline{y}^k$

$$[y_1^k, y_2^k, y_3^k, \ldots]$$

where n, k, j and y are integers greater or equal to 1 (n, k, j, y ≥ 1).

Reasons For Allowance

6. Claims 41-80, renumbered as 1-40, are allowed. The following is an examiner's statement of reasons for allowance:

As per independent claims 1 and 52, the prior arts of record have failed to provide disclosure or support for the unique feature wherein "*the switching units are configured to be controllable such that an input signal present at the internal input of a switching unit, in dependence on a control signal of the switching unit, is forwarded either unchanged to the internal input of the switching unit arranged downstream or to the circuit output and/or are fed back to an internal input of a switching unit arranged upstream, or are combined with the test signal in each case present at the external input and the combination value determined from*

this combination is forwarded to the internal input of the switching unit in each case arranged downstream or to the circuit output and/or is fed back to the internal input of one of the switching units arranged upstream".

As per independent claims 62 and 76, the prior arts of record have failed to provide disclosure or support for the unique feature wherein "*if at least one errored signature has been determined, carrying out the following processes: performing k successive test runs, wherein in each case only those data, present at the external input, of the n datastreams in the jth run are included in the compacting in the electrical diagnostic circuit if the binary coefficient* $a_{i,j}$ *of the equations for determining the control points of a linear separable error-correcting code with n information points* $u_1, ..., u_n$ *and with k control points* $v_1, ..., v_k$ *is equal to one, the k control points* $v_1, ..., v_k$ *being determined by the k binary equations*

$$v_1 = a_{1,1}\, u_1 \oplus \ldots \oplus a_{1,n} u_n$$

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$$v_1 = a_{k,1} u_1 \oplus \ldots \oplus a_{k,n} u_n$$

from the n information points.

determining the errored elements in the n datastreams, particularly the errored

scan cells of the diagnosed integrated circuit from the deviations of observed output signatures $\underline{y}^b$ output by the electrical diagnostic circuit at its output in the k test runs

$$[y_1^b, y_2^b, y_3^b, \ldots]$$

from the corresponding correct output signatures $\underline{y}^k$

$$[y_1^k, y_2^k, y_3^k, \ldots]$$

where n, k, j and y are integers greater or equal to 1 (n, k, j, y ≥ 1)."

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Hill et al (US 7,644,333 B2) teaches a method and apparatus for testing an integrated circuit using built-in-self-test techniques.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guerrier Merant whose telephone number is (571) 270-1066. The examiner can normally be reached on M. - Friday. 8:30 AM - 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin L. Ellis can be reached on (571) 272-4205. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Guerrier Merant
05/21/10

/Kevin L Ellis/
Supervisory Patent Examiner, Art Unit 2117